Remarks

Allowance of all claims is respectfully requested. Claims 1-9 & 11-15 remain pending.

Initially, Applicants gratefully acknowledge the indication of allowability of claim 6 if rewritten into independent form including all the limitations of the base claim and any intervening claims. Presently, this dependent claim has not been rewritten into independent form since the amended independent claim from which it depends is believed to be in condition for allowance for the reasons stated below.

By this paper, claims 1 & 9 are amended (and claim 10 is canceled) to more clearly point out and distinctly claim certain aspects of the present invention. These claim amendments are submitted in a *bona fide* attempt to further prosecution of the application. Support for the amended language can be found throughout the application as filed. For example, reference paragraphs [0024], [0025], and [0029]-[0031], as well as the figures. No new matter is added to the application by any amendment presented.

Double Patenting Rejection:

As noted above, Applicants respectfully request entry of the Terminal Disclaimer submitted herewith and withdrawal of the provisional rejection to claims 1, 2, 7-10, 12 and 13 under the judicially created doctrine of obviousness-type double patenting over claims 26, 28, 32, 45 & 56 of commonly assigned, co-pending application no. 09/985,693.

In view of the submission of the Terminal Disclaimer, withdrawal of the provisional, obviousness-type double patenting rejection is respectfully requested.

35 U.S.C. §102:

In the Office Action, claims 1-5 & 7-11 were rejected under 35 U.S.C. §102(b) as being anticipated by Burnette (U.S. Patent No. 5,956,606; hereinafter Burnette). Additionally, claims 1-5 & 7-14 were rejected under 35 U.S.C. §102(b) as being anticipated by Kodama et al. (U.S. Patent No. 5,878,942; hereinafter Kodama), and claims 1-5 & 7-15 were rejected under 35 U.S.C. §102(e) as being anticipated by Fallon et al. (U.S. Patent No. 6,759,738 B1; hereinafter Fallon). Each of these rejections is respectfully, but most strenuously, traversed to any extent deemed applicable to the amended claims presented herewith and reconsideration thereof is requested.

Current solder bump array deposition technologies require an expensive and time consuming mask alignment process. This alignment process becomes increasingly difficult and costly as the solder bump size and pitches decrease. To realize the full advantages of multi-chip stack technology, very high solder bump interconnect density is needed. Unfortunately, the multi-chip stack structure the expensive and inherent technology limitations associated with current solder bump array technologies. Applicants' claimed method of joining is designed to address these inherent limitations by providing a self-aligning interconnect structure.

As recited in amended claim 1, for example, Applicants' invention comprises a method of joining which includes providing a first substrate and a second substrate, and providing first solder bumps and second bumps offset between the first substrate and the second substrate to connect the first substrate and the second substrate. The second solder bumps have at least a portion which melts at a substantially lower temperature than the first solder bumps. The joining method further includes reflowing the second solder bumps to align the first solder bumps between the first substrate and the second substrate, the alignment occurring before the first solder bumps are reflowed. Applicants respectfully submit that this process recited in amended claim 1 is clearly distinct from the teachings and suggestions of Burnette, Kodama and Fallon.

It is well settled that there is no anticipation of a claim unless a single prior art reference discloses: (1) all the same elements of the claimed invention; (2) found in the same situation as the claimed invention; (3) united in the same way as the claimed; and (4) in order to perform the identical function as the claimed invention. In this instance, Burnette, Kodama and Fallon each fail to disclose various aspects of Applicants' invention as recited in amended independent claim 1, and as a result, do not anticipate (or even render obvious) Applicants' invention.

Burnette describes a method for bumping and packaging semiconductor die. An electrical interconnect structure is disclosed including a first component (300), a second component (320), and an electrical interconnect electrically and mechanically interconnecting the first component to the second component. The electrical interconnect includes a first solder sphere (314) and a second solder sphere (318) stacked on each other. (See Abstract.)

Initially, Applicants note that Burnette does not discuss the problem addressed by the present invention (i.e., how to achieve better alignment of fine pitched solder bumps). Rather, Burnette is addressing providing improved interconnect structures for both first-level and second-level packaging. As shown in the figures of Burnette, the interconnection bumps (110, 114, 314, 318) align vertically and comprise structures designed to enhance the electrical connection of the substrates (104, 112, 300, 320).

In contrast, Applicants' amended claim 1 characterizes the first solder bumps and the second solder bumps as being offset between the first substrate and the second substrate. Clearly, the first solder bumps and second solder bumps in Burnette are vertically aligned, and would therefore not be offset (i.e., horizontally displaced) between the first substrate and the second substrate.

Further, Applicants recite reflowing of the second solder bumps to align the first solder bumps between the first substrate and the second substrate. This alignment of the first solder bumps occurs before the first solder bumps are reflowed. Applicants respectfully submit that Burnette does not teach or suggest this functionality. There is no alignment in Burnette of first solder bumps disposed between the first and second substrate and offset from the second solder bumps (which are reflowed). In Applicants' invention, the reflowing of the second solder bumps provides a further level of alignment between the first and second substrates prior to reflowing of the first solder bumps.

For at least the above reasons, Applicants respectfully submit that amended independent claim 1 patentably distinguishes over the teachings of Burnette. Reconsideration and withdrawal of the rejection based thereon is therefore requested.

Kodama describes methods and apparatus for performing soldering while the chip is held by a head under melted solder conditions. Solder bumps 3 are formed on the chip 1, and they are opposite to terminals 11 on a mounting board 10. Furthermore, a heating block 21 is located at the back of the chip, and it raises the temperature of the solder bumps 3 on the chip to a melting point by heating the chip back by conduction. Preferably, another heating block 22 is located at the back of the mounting board 10. Soldering is performed by bringing the solder bumps 3 into contact with terminals 11 while the solder is melted. (See Abstract of Kodama.)

Applicants again respectfully submit that a careful reading of Kodama fails to uncover any teaching or suggestion of their recited first solder bumps and second solder bumps offset between the first substrate and the second substrate to connect the first substrate and the second substrate. The first and second solder bumps (30, 31) shown in Figs. 14 & 16 are vertically aligned between chip substrates 1 & 10.

Still further, Applicants recite reflowing the second solder bumps to align the first solder bumps between the first substrate and the second substrate. This alignment occurs before the first solder bumps are reflowed. Applicants respectfully submit that Kodama does not teach or suggest this functionality. There is no alignment of the first solder bumps with reflowing of the second solder bumps occurring in Kodama.

For the above reasons, Applicants respectfully submit that amended independent claim 1 patentably distinguishes over the teachings of Kodama. Reconsideration and withdrawal of the rejection based thereon is therefore requested.

Fallon describes systems interconnected by bumps of joining material. Joining material paste if forced through holes in a screen onto an area array of the contacts on the substrate when the screen is biased against the substrate as the paste is heated and cooled to transfer the joining material onto the contacts. Alternatively, joining material paste is forced onto the screen and then a substrate is placed onto the screen with an area array of bump contacts of the substrate in contact with the solder paste. The solder paste is heated and cooled to transfer the material onto the bumps. The joining material may be a solder paste, conductive adhesive paste, or transient liquid bond paste. As shown in Figs. 32 & 35, the first and second solder bumps (750, 712), as characterized in the Office Action, again align vertically between the chip substrates.

Applicants respectfully submit that Fallon fails to teach or suggest the presence of first solder bumps and second solder bumps offset between the first substrate and the second substrate to connect the first substrate and the second substrate. As noted, the solder bumps in Fallon vertically align in a manner similar to those in Burnette and Kodama.

Additionally, Applicants' recite in amended claim 1 the reflowing of the second solder bumps to align the first solder bumps between the first substrate and the second substrate. This alignment of the first solder bumps occurs before the first solder are reflowed. No similar processing is believed taught or suggested by Fallon. Applicants respectfully submit that Fallon (like Burnette and Kodama) do not teach or suggest Applicants' reflowing the second solder bumps to provide another level of alignment between the first and second substrates (which facilitates precise alignment of the first solder bumps) before the first solder bumps are melted.

For all of the above reasons, Applicants respectfully submit that independent claim 1 patentably distinguishes over the teachings of Fallon. Reconsideration and withdrawal of the rejection based thereon is therefore also requested.

The dependent claims are believed patentable for the same reasons as the independent claim from which they directly or ultimately depend, as well as for their own additional characterizations.

The application is believed to be in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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